A38, cont'd -; and

Page **116, line 17**, after "Fig. 37" insert --and Fig. 44--

## REMARKS

Claims 1-27 are pending in this application. For purposes of completeness, the specification has been amended to include additional materials intended to clarify and complete the text pertaining to the disclosed invention. No new matter has been introduced since the additional materials are only intended to describe the same invention from different perspectives, in order to assist the Examiner to understand and expedite compacted prosecution. Figures 38-44 are likewise added to illustrate the disclosed invention from different perspectives. For the Examiner's convenience, a copy of the substitute specification is attached herewith as Exhibit A. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at (703) 312-6600.

No fees have been incurred. Please charge any shortage in fees due in connection with the filing of this paper, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (503.39864X00).

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# EXHIBIT A

# SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

[0001]

## BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a manufacturing method thereof and more particularly to a semiconductor device and a manufacturing method thereof that a semiconductor element has at least a stress cushioning layer and a semiconductor protective layer, and the end faces of these layers are positioned inside the cutting scribe lines formed on a semiconductor wafer, and the range of the surface at the end of the semiconductor element from the end face to the inside of the scribe line is exposed.

[0002]

Recently, there are increasing requests for miniaturization and high performance in various electronic elements and in association with those requests, also for a semiconductor device using electronic elements, speeding up of information processing as well as high density packing and high density assembly are required. Namely, in correspondence with these requests, a semiconductor device is moving from the pin insertion type to the

surface mounting type so as to increase the mounting density and to correspond to multi-pin, various packages from a DIP (dual inline package) to a QFP (quad flat package) or a PGA (pin grid array) have been developed.

[0003]

However, in the QFP type, the connection lead wires for connecting with the mounting substrate are centralized in the peripheral part of the package and the connection lead wires themselves are thin and deformable, so that as the number of pins increases, mounting is getting hard. In the PGA type, the terminals to be connected to the mounting substrate are thin and long and a considerable number of terminals are centralized, so that high speed processing of information is difficult from the viewpoint of characteristics and moreover the PGA is of a pin insertion type, so that surface mounting is not available and it is disadvantageous in high density assembly.

[0004]

Recently, to solve various problems of these packages and realize a semiconductor corresponding to high speed processing of information, a BGA (ball grid array) package having a stress cushioning layer

between the semiconductor element and the substrate with a wiring circuit formed and a bump electrode which is an external terminal on the mounting substrate surface side of the substrate with the wiring circuit formed has been developed and the contents thereof are disclosed in the specification of USP 5148265. In the package described in the specification of USP 5148265, since the terminals to be connected to the mounting substrate are ball-shaped solder, the lead wires are free of deformation unlike the QFP type and since the terminals are scattered overall the mounting surface, the pitch between the terminals is large and surface mounting can be carries out easily. The bump electrode which is an external terminal is shorter in length than that of the PGA type, so that the inductance component is decreased, and the information processing speed is increased, and high speed processing of information is made possible.

[0005]

On the other hand, recently, in association with wide spread of portable information terminals, there are increasing requests for miniaturization and high density assembly of a semiconductor device. Therefore, recently, a CSP (chip scale package) that the package size is almost equal to the chip size has been

developed and for example, various types of CSPs are disclosed in "Nikkei Microelement" (pp. 38-64) issued by Nikkei BP, Ltd. (February 1998). CSPs disclosed in it are manufactured in such a way that semiconductor elements cut into pieces are bonded onto a polyimide or ceramics substrate with a wiring layer formed, and then the wiring layer and semiconductor elements are electrically connected by a means such as wire bonding, single point bonding, gang bonding, or bump bonding, and the connections are sealed with resin, and finally external terminals such as solder bumps are formed.

[0006]

In Japanese Patent Application Laid-Open 9-232256 and Japanese Patent Application Laid-Open 10-27827, methods for mass-producing CSPs are disclosed. The manufacturing methods form bumps on a semiconductor wafer, electrically connect a wiring substrate via the bumps, seals the connections with resin, forms external electrodes on the wiring substrate, and finally cuts the semiconductor wafer into pieces, thus manufactures individual semiconductor devicees. Furthermore, "Nikkei Microelement" (p. 164 to p. 167) issued by Nikkei BP, Ltd. (April 1998) discloses another manufacturing method for mass-producing CSPs. This manufacturing method forms bumps by plating on a

semiconductor wafer, seals the part other than the bumps with resin, forms external electrodes in the bumps, then cuts the semiconductor wafer into pieces, and manufactures individual semiconductor devicees. In addition to it, Japanese Patent Application Laid-Open 10-92865 discloses a semiconductor device of a type that a resin layer for cushioning stress is installed between external electrodes and semiconductor elements. Individual semiconductor devicees are manufactured by processing in units of semiconductor wafers in a batch and finally cutting each semiconductor wafer into pieces.

[0007]

The aforementioned semiconductor devicees (semiconductor package) of a type that a plurality of resin layers and external electrodes are formed in units of semiconductor wafers in a batch, and then each semiconductor wafer is cut (diced) into pieces, thereby individual semiconductor devicees are manufactured has a constitution that the interfaces of a plurality of resin layers sequentially formed on each semiconductor wafer are exposed on the end face of each semiconductor package, so that when large mechanical stress is applied to the interfaces of the plurality of resin layers at the time of dicing of the

semiconductor wafer or when large thermal stress is applied to the interfaces of the plurality of resin layers due to sudden temperature changes at the time of mounting of the semiconductor package, the stress is centralized to the interfaces between the semiconductor element exposed on the end face of the semiconductor package and the plurality of resin layers, thus one or more of the plurality of resin layers are peeled off and the semiconductor package may be damaged.

[0008]

As mentioned above, such a known semiconductor device cannot always obtain high reliability and it is difficult to obtain a high manufacture yield rate.

[0009]

The present invention was developed with the foregoing technical background in view and is intended to provide a semiconductor device and a manufacturing method thereof having high reliability and a satisfactory manufacturing yield rate that the constituent part to which concentrated stress is applied at the time of cutting of a semiconductor wafer and at the time of mounting of a semiconductor device is improved so as to withstand the stress and occurrences of damage of semiconductor devicees due to

applied stress are greatly reduced.

[0010]

To accomplish the above object, the semiconductor device of the present invention has semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along the cutting scribe line, a stress cushioning layer installed on the semiconductor elements, a lead wire portion extending from the electrode pad to the top of the stress cushioning layer through an opening formed in the stress cushioning layer on the electrode pad, external electrodes arranged on the lead wire portion on the top of the stress cushioning layer, and a conductor protective layer installed on the stress cushioning layer excluding the external electrode arranged portion and on the conductor portion and the stress cushioning layer, lead wire portion, conductor protective layer, and external electrodes have a means for forming each end face on the end surface of the semiconductor elements inside the cutting scribe line and exposing the range from the end face on the end surface of the semiconductor elements to the inside of the scribe line.

[0011]

To accomplish the above object, the semiconductor device of the present invention has semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along the cutting scribe line, a semiconductor element protective layer installed on the semiconductor elements, a stress cushioning layer installed on the semiconductor element protective layer, a first opening formed in the semiconductor element protective layer on the electrode pad, a second opening formed in the stress cushioning layer on the electrode pad, a lead wire portion extending to the top of the stress cushioning layer through the first opening and second opening respectively from the electrode pad, external electrodes arranged on the lead wire portion on the top of the stress cushioning layer, and a conductor protective layer installed on the stress cushioning layer excluding the external electrode arranged portion and on the conductor portion and the semiconductor element protective layer, stress cushioning layer, lead wire portion, conductor protective layer, and external electrodes have a means for forming each end face on the end surface of the semiconductor elements inside the cutting scribe line and exposing the range from the end face on the end

surface of the semiconductor elements to the inside of the scribe line.

[0012]

To accomplish the above object, the semiconductor device manufacturing method of the present invention has a means for manufacturing a semiconductor device through a first step of forming a plurality of semiconductor elements having an integrated circuit and an electrode pad on the circuit forming surface of a semiconductor wafer, a second step of forming a stress cushioning layer on a plurality of semiconductor elements, a third step of forming an opening in the electrode pad of the stress cushioning layer and forming a notch wider than the width of the scribe line in the stress cushioning layer on the cutting scribe line of the semiconductor wafer, a fourth step of forming a lead wire portion extending from the electrode pad to the stress cushioning layer via the opening, a fifth step of forming a conductor protective layer which covers the stress cushioning layer and lead wire portion and has an external electrode connection window portion on the lead wire portion and a notch at the position corresponding to the notch of the stress cushioning layer, a sixth step of forming an external electrode in the external

electrode connection window portion, and a seventh step of cutting the semiconductor wafer along the cutting scribe line and obtaining a plurality of semiconductor devicees in minimum units.

[0013]

To accomplish the above object, the semiconductor device manufacturing method of the present invention has a means for manufacturing a semiconductor device through a first step of forming a plurality of semiconductor elements having an integrated circuit and an electrode pad on the circuit forming surface of a semiconductor wafer, a second step of forming a semiconductor element protective layer on a plurality of semiconductor elements, a third step of forming a first opening in the electrode pad of the semiconductor element protective layer and forming a notch wider than the width of the scribe line in the semiconductor element protective layer on the cutting scribe line of the semiconductor wafer, a fourth step of forming a stress cushioning layer on the semiconductor element protective layer, a fifth step of forming a second opening in the electrode pad of the stress cushioning layer and forming a notch at the position corresponding to the notch of the semiconductor element protective layer in the stress

cushioning layer on the cutting scribe line of the semiconductor wafer, a sixth step of forming a lead wire portion extending from the electrode pad to the stress cushioning layer via the first and second openings, a seventh step of forming a conductor protective layer which covers the stress cushioning layer and lead wire portion and has an external electrode connection window portion on the lead wire portion and a notch at the position corresponding to the notch of the stress cushioning layer, an eighth step of forming an external electrode in the external electrode connection window portion, and a ninth step of cutting the semiconductor wafer along the cutting scribe line and obtaining a plurality of semiconductor devicees in minimum units.

[0014]

According to each means mentioned above, each end face of the stress cushioning layer and conductor protective layer or each end face of the semiconductor element protective layer, stress cushioning layer, and conductor protective layer in the end face area of each semiconductor element is formed so as to be positioned inside the semiconductor wafer cutting scribe line and exposed within the range from the end face of each semiconductor element to the inside of

the scribe line, so that when a semiconductor wafer is to be cut along the semiconductor wafer cutting scribe line, the semiconductor wafer can be cut by surely recognizing the positioning marks put on the semiconductor wafer and defective semiconductor packages due to a displacement of the cutting position of each obtained semiconductor device can be eliminated.

[0015]

Further, according to each means mentioned above, when each semiconductor device is to be obtained by cutting a semiconductor wafer, the cut portion of each semiconductor device is formed in a single-layer structure only of a semiconductor element and even if mechanical stress is generated at the time of cutting of the semiconductor wafer, the mechanical stress is just applied to the single-layer structure, so that a plurality of resin layers will not be peeled off by the mechanical stress.

[0016]

Furthermore, according to each means mentioned above, when each semiconductor device is to be mounted, even if thermal stress is generated due to great changes of the environmental temperature and the thermal stress is applied to a plurality of resin

layers, large mechanical stress is not applied to the plurality of resin layers when the semiconductor wafer is cut and the plurality of resin layers are little damaged, so that the plurality of resin layers will be peeled off not at all or very little due to thermal stress.

[0017]

As mentioned above, according to each means mentioned above, semiconductor devicees are damaged not at all or very little due to application of mechanical stress and thermal stress, and the reliability of semiconductor devicees can be enhanced, and the production yield rate of semiconductor devicees can be increased.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is cross sectional view showing the constitution of the essential section of the semiconductor device of the first embodiment of the present invention.

Fig. 2 is cross sectional view showing the constitution of the essential section of the semiconductor device of the second embodiment of the present invention.

Fig. 3 is cross sectional view showing the

constitution of the essential section of the semiconductor device of the third embodiment of the present invention.

Fig. 4 is cross sectional view showing the constitution of the essential section of the semiconductor device of the fourth embodiment of the present invention.

Fig. 5 is cross sectional view showing the constitution of the essential section of the semiconductor device of the fifth embodiment of the present invention.

Fig. 6 is cross sectional view showing the constitution of the essential section of the semiconductor device of the sixth embodiment of the present invention.

Fig. 7 is cross sectional view showing the constitution of the essential section of the semiconductor device of the seventh embodiment of the present invention.

Fig. 8 is cross sectional view showing the constitution of the essential section of the semiconductor device of the eighth embodiment of the present invention.

Fig. 9 is cross sectional view showing the constitution of the essential section of the

semiconductor device of the ninth embodiment of the present invention.

Fig. 10 is cross sectional view showing the constitution of the essential section of the semiconductor device of the tenth embodiment of the present invention.

Fig. 11 is cross sectional view showing the constitution of the essential section of the semiconductor device of the eleventh embodiment of the present invention.

Fig. 12 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twelfth embodiment of the present invention.

Fig. 13 is cross sectional view showing the constitution of the essential section of the semiconductor device of the thirteenth embodiment of the present invention.

Fig. 14 is cross sectional view showing the constitution of the essential section of the semiconductor device of the fourteenth embodiment of the present invention.

Fig. 15 is cross sectional view showing the constitution of the essential section of the semiconductor device of the fifteenth embodiment of

the present invention.

Fig. 16 is cross sectional view showing the constitution of the essential section of the semiconductor device of the sixteenth embodiment of the present invention.

Fig. 17 is cross sectional view showing the constitution of the essential section of the semiconductor device of the seventeenth embodiment of the present invention.

Fig. 18 is cross sectional view showing the constitution of the essential section of the semiconductor device of the eighteenth embodiment of the present invention.

Fig. 19 is cross sectional view showing the constitution of the essential section of the semiconductor device of the nineteenth embodiment of the present invention.

Fig. 20 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twentieth embodiment of the present invention.

Fig. 21 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-first embodiment of the present invention.

Fig. 22 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-second embodiment of the present invention.

Fig. 23 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-third embodiment of the present invention.

Fig. 24 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-fourth embodiment of the present invention.

Fig. 25 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-fifth embodiment of the present invention.

Fig. 26 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-sixth embodiment of the present invention.

Fig. 27 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-seventh embodiment of the present invention.

Fig. 28 is cross sectional view showing the

constitution of the essential section of the semiconductor device of the twenty-eighth embodiment of the present invention.

Fig. 29 is cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-ninth embodiment of the present invention.

Fig. 30 is cross sectional view showing the constitution of the essential section of the semiconductor device of the thirtieth embodiment of the present invention.

Fig. 31 is cross sectional view showing the constitution of the essential section of the semiconductor device of the thirty-first embodiment of the present invention.

Fig. 32 is cross sectional view showing the constitution of the essential section of the semiconductor device of the thirty-second embodiment of the present invention.

Fig. 33 is cross sectional view showing the constitution of the essential section of the semiconductor device of the thirty-third embodiment of the present invention.

Fig. 34 is cross sectional view showing the constitution of the essential section of a

semiconductor device as a first comparison example.

Fig. 35 is cross sectional view showing the constitution of the essential section of a semiconductor device as a second comparison example.

Fig. 36 is cross sectional view showing the constitution of the essential section of a semiconductor device as a third comparison example.

Fig. 37 is cross sectional view showing the constitution of the essential section of a semiconductor device as a fourth comparison example.

Fig. 38 is a view showing a semiconductor device according to first, third, forth, sixth, seventh and ninth embodiments of this invention and illustrates the structure of its substantial part.

Fig. 39 is a view showing a semiconductor device according to second, fifth and eighth embodiments of this invention and illustrates the structure of its substantial part.

Fig. 40 is a view showing a semiconductor device according to tenth, fourteenth, sixteenth, seventeenth, eighteenth, twenty-second, twenty-sixth, twenty-eighth, twenty-ninth, thirtieth, thirty-second and thirty-third embodiments of this invention and illustrates the structure of its substantial part.

Fig. 41 is a view showing a semiconductor device

according to eleventh, thirteenth, nineteenth, twenty-first, twenty-third and twenty-fifth embodiments of this invention and illustrates the structure of its substantial part.

Fig. 42 is a view showing a semiconductor device according to twelfth, twentieth, twenty-forth and thirty-first embodiments of this invention and illustrates the structure of its substantial part.

Fig. 43 is a view showing a semiconductor device according to fifteenth and twenty-seventh embodiments of this invention and illustrates the structure of its substantial part.

Fig. 44 is a view showing a semiconductor device which constitutes first, second, third and forth comparison examples and illustrates the structure of its substantial part.

[0018]

DETAILED DESCRIPTION OF THE INVENTION

The embodiments of the semiconductor device and manufacturing method thereof of the present invention will be explained hereunder with reference to the accompanying drawings.

[0019]

Fig. 1 is a cross sectional view showing the

constitution of the essential section of the semiconductor device of the first embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a first embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 1 shows a sectional view taken along lines A-B in Fig. 38.

[0020]

In Fig. 1 and Fig. 38, numeral 1 indicates a semiconductor element, 1(1) an exposed end face of the semiconductor element 1, 2 an electrode pad, 3 a stress cushioning layer, 3(1) an opening formed in the stress cushioning layer 3, 4 a lead wire portion, 5 a conductor protective layer, 5(1) a plurality of windows installed in the conductor protective layer 5, and 6 an external electrode.

[0021]

The semiconductor element 1 has the electrode pad 2 and an integrated circuit portion not shown in the drawing which are arranged on one side thereof and the exposed end face 1(1). The stress cushioning layer 3 is formed on one side of the semiconductor element 1 and has the opening 3(1) on the electron pad 2 and a slit (no drawing No. is assigned) reaching the bottom on the end face 1(1). The lead wire portion 4 is

formed within the range from the electrode pad 2 to a part of the stress cushioning layer 3 via the opening 3(1). The conductor protective layer 5 is formed on the stress cushioning layer 3 including the lead wire portion 4 and has a plurality of windows 5(1) on a part of the lead wire portion 4 and a slit (no drawing No. is assigned) reaching the bottom of the conductor protective layer 5 at the position corresponding to the slit of the stress cushioning layer 3 on the end face 1(1). The external electrodes 6 are arranged on the lead wire portion 4 via each of the window portions 5(1).

[0022]

In this case, the end face of the stress cushioning layer 3 obtained by forming of the slit and the end face of the conductor protective layer 5 obtained by forming of the slit are positioned on the same surface and the exposed end face 1(1) is formed within the range from the end face of the semiconductor element 1 to the end face of the stress cushioning layer 3 and the end face of the conductor protective layer 5 positioned on the same surface. The end face of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are positioned slightly inside the cutting scribe line

formed on a semiconductor wafer (not shown in the drawing) which will be described later.

[0023]

Next, the semiconductor device manufacturing method of the first embodiment will be described. A plurality of semiconductor devicees are manufactured at the same time by cutting a semiconductor wafer and on the semiconductor wafer, positioning marks (not shown in the drawing) are formed at the intersections of the scribe lines which are a cutting portion and semiconductor devicees are formed respectively one side of the semiconductor wafer enclosed by the positioning marks, and then the semiconductor wafer is cut along the positioning marks, thereby a plurality of semiconductor devicees are manufactured.

[0024]

Firstly, positioning marks of aluminum (Al) indicating an intersection of scribe lines are formed on one side of a semiconductor wafer of silicon (Si) and in the areas enclosed by the positioning marks, the electrode pads 2 of aluminum (Al) are formed respectively and an integrated circuit portion (not shown in the drawing) is formed.

[0025]

Next, on one side of the semiconductor wafer with

the positioning marks and electrode pads 2 formed, the stress cushioning layer 3 including the opening 3(1) having a gently-inclined rising portion is formed using the mask printing method. In this case, the printing mask to be used by the mask printing method has the same structure as that of the printing mask used for solder paste printing in a printed circuit board and a so-called contact print for positioning and closely adhering a semiconductor wafer pattern and a printing mask and executing squeeze printing in this state is used. During printing, the whole squeeze surface of the printing mask is coated with paste at the first squeezing, and the opening of the printing mask is filled at the second squeezing, and excessive paste is removed, and then the printing mask is removed from the semiconductor wafer, and the mask print is completed. Thereafter, the semiconductor wafer with paste print-coated is heated stepwise using a hot plate or a heating oven, and the print-coated paste is hardened, and the stress cushioning layer 3 having the opening 3(1) is formed.

[0026]

The material to be used to form the stress cushioning layer 3 is a pasty polyimide material and is hardened by heating after print-coating. The pasty

polyimide material has satisfactory print-coating characteristics such as viscosity of 530 Pa-s and a thixotropy factor of 2.8. When such a pasty polyimide material is used, the wetting spread is made smaller and the stress cushioning layer 3 having the opening 3(1) as shown in Fig. 1 can be formed. When a stress cushioning layer 3 having a necessary thickness cannot be obtained by one mask printing, by repeating print-coating and hardening of the coated material several times, a predetermined thickness can be obtained.

[0027]

In this case, when a pasty polyimide material is used as a forming material of the stress cushioning layer 3 and a metal mask with a thickness of 65 μm is used as a printing mask, by print-coating and hardening of the coated material two times, a stress cushioning layer 3 with a thickness of 50 μm can be obtained. The hardening conditions in this case are that the material is print-coated firstly, heated on a hot plate at 100°C for 10 minutes, heated and hardened at 150°C for 10 minutes, then print-coated secondarily, heated on the hot plate at 200°C for 25 minutes, and then heated and hardened in a thermostatic chamber at 250°C for 60 minutes.

[0028]

In the first embodiment, the stress cushioning layer 3 is formed using a pasty polyimide material. However, any low elastic resin material can ensure the viscoelastic characteristics necessary for mask printing and withstand this manufacturing process from the viewpoint of characteristics, it may be used.

[0029]

Next, a scribe line with a width of 200 μm formed on a semiconductor wafer by laser processing using a carbon dioxide laser is exposed. In this case, a slit with a width of 400 μm reaching the bottom of the stress cushioning layer 3 is formed in the stress cushioning layer 3 formed on the end surface 1(1) and the positioning marks of the semiconductor wafer formed on the end surface 1(1) are exposed via this slit.

[0030]

Then, a chromium (Cr) film with a thickness of 500 Å is deposited on the stress cushioning layer 3 including the electrode pad 2 and a copper (Cu) film with a thickness of 0.5 μm is deposited on it. A negative type photosensitive resist is spin-coated on the obtained deposited film, prebaked, exposed, and developed and a resist wiring pattern with a thickness of 15 μm is formed. A copper (Cu) film with a

thickness of 10 μm is formed by electroplating inside the formed wiring pattern and a nickel (Ni) film with a thickness of 2 μm is formed on it by electroplating. Thereafter, the resist is peeled off using a release liquid, and the copper (Cu) film among the deposited films is etched by an ammonium persulfate/sulfuric acid series solution, and furthermore, the chromium (Cr) film among the deposited films is etched by a potassium permanganate series solution, and the lead wire portion 4 is formed.

[0031]

When the lead wire portion 4 formed at this point of time is evaluated on suitability, no unsuitable (defective) lead wire portions are found at all among all the evaluated ones.

[0032]

Next, the stress cushioning layer 3 including the lead wire portion 4 is coated with photosensitive solder resist varnish by screen printing, and the coated film is dried at 80°C for 20 minutes, exposed and developed using a predetermined pattern, and heated and hardened at 150°C for one hour, and the conductor protective layer 5 is formed. The formed conductor protective layer 5 has a plurality of window portions 5(1) on a part of the lead wire portion 4 and

a slit (no drawing number is assigned) reaching the bottom of the conductor protective layer 5 at the position coinciding with the slit forming position of the stress cushioning layer 3 on the scribe line.

[0033]

Next, a gold (Au) plating film with a thickness of 0.1 μm is formed by replacement plating on the nickel (Ni) film of the lead wire portion 4 which is exposed via the windows 5(1). Thereafter, flux is coated on the gold (Au) plating film using a metal mask, and solder balls of Sn-Ag-Cu series with a diameter of about 0.35 mm are put on it, and the solder balls are heated in an infrared reflow furnace at 260°C for 10 seconds, and the external electrodes 6 are formed.

[0034]

Finally, by checking the positioning marks formed on the end surface 1(1) of the semiconductor element 1, that is, on the semiconductor wafer by transmission, the semiconductor wafer is cut by a dicing saw with a thickness of 0.2 mm along the scribe line and a plurality of semiconductor devicees are manufactured.

[0035]

The semiconductor devicees of the first embodiment manufactured by this method are subjected to the appearance inspection immediately after dicing and it

is found that the end area of the semiconductor element 1 including the plural-layer forming portion is not damaged at all during dicing and there are no defective semiconductor packages produced at all.

[0036]

Samples of a predetermined number are extracted from the semiconductor devicees of the first embodiment manufactured in this way, and a temperature test is executed for each of the extracted samples that a temperature cycle of conditioning at -55°C for 10 minutes and conditioning at 125°C for 10 minutes is repeated 1000 times, and each sample is subjected to the appearance inspection after the temperature test is executed, and it is found that the plural-layer forming portion of the end area of the semiconductor element 1 is not damaged during dicing, thus the interface of the plural-layer forming portion is not peeled off and no defective samples are generated at all.

[0037]

Fig. 2 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the second embodiment of the present invention. Also, Fig. 39 is a view showing a semiconductor device according to a second embodiment

of this invention and illustrates the structure of its substantial part. Further, Fig. 2 shows a sectional view taken along lines A-B in Fig. 39.

[0038]

In Fig. 2 and Fig. 39, numeral 3(2) indicates an exposed end surface of the stress cushioning layer 3 and with respect to the other numerals, the same numeral is assigned to each of the same components as those shown in Fig. 1.

[0039]

The constituent difference between the aforementioned semiconductor device of the first embodiment (hereinafter, referred to as the first embodiment device) and the semiconductor device of the second embodiment (hereinafter, referred to as the second embodiment device) is only a point that with respect to the constitution of the slit portion of the stress cushioning layer 3 on the end surface 1(1) of the semiconductor element 1 and the slit portion of the conductor protective layer 5, the first embodiment device is structured so that the end face of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are installed on the same plane, while the second embodiment device is structured so that the end face of the conductor

protective layer 5 is positioned on the inside compared with the end face of the stress cushioning layer 3 and the exposed end surface 3(2) is installed on the stress cushioning layer 3 and there are no other constituent differences between the first embodiment device and the second embodiment device. Therefore, additional explanation on the constitution of the second embodiment device will be omitted.

[0040]

The manufacturing method of the second embodiment device is the same as the manufacturing method of the first embodiment device, so that the explanation on the manufacturing method of the second embodiment device will be also omitted.

[0041]

The second embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective

samples at all.

[0042]

Fig. 3 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the third embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a third embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 3 shows a sectional view taken along lines A-B in Fig. 38.

[0043]

In Fig. 3 and Fig. 38, the same numeral is assigned to each of the same components as those shown in Fig. 1.

[0044]

The constituent difference between the aforementioned semiconductor device of the first embodiment (hereinafter, referred to as the first embodiment device again) and the semiconductor device of the third embodiment (hereinafter, referred to as the third embodiment device) is only a point that with respect to the constitution of the slit portion of the stress cushioning layer 3 and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the first embodiment

device is structured so that the end face of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are installed on the same plane, while the third embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside compared with the end face of the stress cushioning layer 3 and the conductor protective layer 5 of the outside part reaches the end surface 1(1) and there are no other constituent differences between the first embodiment device and the third embodiment device. Therefore, additional explanation on the constitution of the third embodiment device will be omitted.

[0045]

The manufacturing method of the third embodiment device is the same as the manufacturing method of the first embodiment device, so that the explanation on the manufacturing method of the third embodiment device will be also omitted.

[0046]

The third embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance

inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0047]

Fig. 4 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the fourth embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a forth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 4 shows a sectional view taken along lines A-B in Fig. 38.

[0048]

In Fig. 4 and Fig. 38, the same numeral is assigned to each of the same components as those shown in Fig. 1.

[0049]

The constituent difference between the aforementioned semiconductor device of the first embodiment (hereinafter, referred to as the first embodiment device again) and the semiconductor device of the fourth embodiment (hereinafter, referred to as

the fourth embodiment device) is only a point that with respect to the constitution of the end area of the stress cushioning layer 3 and the end area of the conductor protective layer 5, the first embodiment device is structured so that a slit portion is formed in the stress cushioning layer 3, and a slit portion is also formed in the conductor protective layer 5, and their end faces are installed on the same plane, while the fourth embodiment device is structured so that a tapered portion becoming thinner taperingly toward the end face is formed on the stress cushioning layer 3, and a slit portion is formed in the conductor protective layer 5, and the end (end face) of the tapered portion and the end face of the slit portion are installed on the same plane, and the thickness of the conductor protective layer 5 replenishes to changes in the thickness of the tapered portion and there are no other constituent differences between the first embodiment device and the fourth embodiment device. Therefore, additional explanation on the constitution of the fourth embodiment device will be omitted.

[0050]

As compared with the manufacturing method of the first embodiment device, the manufacturing method of

the fourth embodiment device has only a difference that with respect to the forming means of the stress cushioning layer 3, the manufacturing method of the first embodiment device forms the stress cushioning layer 3 including the opening 3(1) having a gently-inclined rising portion using the mask printing method and then forms a slit portion in the stress cushioning layer 3 by laser processing, while the manufacturing method of the fourth embodiment device forms the stress cushioning layer 3 including the opening 3(1) having a gently-inclined rising portion and a tapered portion becoming thinner taperingly toward the end face using the mask printing method and does not perform the subsequent laser processing for the stress cushioning layer 3 and there are no other differences between the manufacturing method of the first embodiment device and the manufacturing method of the fourth embodiment device. Therefore, additional explanation on the manufacturing method of the fourth embodiment device will be omitted.

[0051]

The fourth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at

all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0052]

Fig. 5 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the fifth embodiment of the present invention. Also, Fig. 39 is a view showing a semiconductor device according to a fifth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 5 shows a sectional view taken along lines A-B in Fig. 39.

[0053]

In Fig. 5 and Fig. 39, the same numeral is assigned to each of the same components as those shown in Figs. 2 and 4.

[0054]

The constituent difference between the aforementioned semiconductor device of the fourth embodiment (hereinafter, referred to as the fourth embodiment device again) and the semiconductor device

of the fifth embodiment (hereinafter, referred to as the fifth embodiment device) is only a point that with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end face of the conductor protective layer 5, the fourth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are installed on the same plane, while the fifth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the inside compared with the end (end face) of the stress cushioning layer 3 and the exposed end surface 3(2) is installed on the stress cushioning layer 3 and there are no other constituent differences between the fourth embodiment device and the fifth embodiment device. Therefore, additional explanation on the constitution of the fifth embodiment device will be omitted.

[0055]

The manufacturing method of the fifth embodiment device is the same as the manufacturing method of the fourth embodiment device except a point that the mask printing method is used for forming the conductor protective layer 5 in stead of the screen printing method, so that the explanation of the manufacturing

method of the fifth embodiment device will be also omitted.

[0056]

The fifth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0057]

Fig. 6 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the sixth embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a sixth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 6 shows a sectional view taken along lines A-B in Fig. 38.

[0058]

In Fig. 6 and Fig. 38, the same numeral is

assigned to each of the same components as those shown in Fig. 4.

[0059]

The constituent difference between the aforementioned semiconductor device of the fourth embodiment (hereinafter, referred to as the fourth embodiment device again) and the semiconductor device of the sixth embodiment (hereinafter, referred to as the sixth embodiment device) is only a point that with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end face of the conductor protective layer 5, the fourth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are installed on the same plane, while the sixth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside compared with the end (end face) of the stress cushioning layer 3 and the conductor protective layer 5 of the outside part reaches the end surface 1(1) and there are no other constituent differences between the fourth embodiment device and the sixth embodiment device. Therefore, additional explanation on the constitution of the sixth embodiment device will be omitted.

[0060]

The manufacturing method of the sixth embodiment device is the same as the manufacturing method of the fourth embodiment device, so that the explanation on the manufacturing method of the sixth embodiment device will be also omitted.

[0061]

The ~~sixth embodiment device manufactured~~ by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0062]

Fig. 7 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the seventh embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a seventh embodiment of this invention and illustrates the structure of its

substantial part. Further, Fig. 7 shows a sectional view taken along lines A-B in Fig. 38.

[0063]

In Fig. 7 and Fig. 38, the same numeral is assigned to each of the same components as those shown in Fig. 4.

[0064]

The constituent difference between the aforementioned semiconductor device of the fourth embodiment (hereinafter, referred to as the fourth embodiment device again) and the semiconductor device of the seventh embodiment (hereinafter, referred to as the seventh embodiment device) is only a point that with respect to the constitution of the end area of the conductor protective layer 5, the fourth embodiment device is structured so that a slit portion is formed in the conductor protective layer 5 and the end face of the conductor protective layer 5 is almost perpendicular to the end surface 1(1), while the seventh embodiment device is structured so that an inclined surface becoming thinner linearly toward the end face of the conductor protective layer 5 is formed and there are no other constituent differences between the fourth embodiment device and the seventh embodiment device. Therefore, additional explanation

on the constitution of the seventh embodiment device will be omitted.

[0065]

When the manufacturing method of the seventh embodiment device is compared with the manufacturing method of the fourth embodiment device, the difference is only a point that with respect to the forming means of the conductor protective player 5, the manufacturing method of the fourth embodiment device forms the conductor protective layer 5 including the opening 3(1) having a gently-inclined rising portion and a slit portion having an end face almost perpendicular to the end surface 1(1) using the screen printing method, while the manufacturing method of the seventh embodiment device forms the conductor protective layer 5 including the opening 3(1) having a gently-inclined rising portion and an inclined surface having a linearly-inclined rising portion using the mask printing method and there are no other differences between the manufacturing method of the fourth embodiment device and the manufacturing method of the seventh embodiment device. Therefore, additional explanation on the manufacturing method of the seventh embodiment device will be omitted.

[0066]

The seventh embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0067]

Fig. 8 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the eighth embodiment of the present invention. Also, Fig. 39 is a view showing a semiconductor device according to an eighth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 8 shows a sectional view taken along lines A-B in Fig. 39.

[0068]

In Fig. 8 and Fig. 39, the same numeral is assigned to each of the same components as those shown in Figs. 5 and 7.

[0069]

The constituent difference between the aforementioned semiconductor device of the seventh embodiment (hereinafter, referred to as the seventh embodiment device again) and the semiconductor device of the eighth embodiment (hereinafter, referred to as the eighth embodiment device) is only a point that with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5, the seventh embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5 are installed on the same plane, while the eighth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the inside compared with the end (end face) of the stress cushioning layer 3 and the exposed end surface 3(2) is installed on the stress cushioning layer 3 and there are no other constituent differences between the seventh embodiment device and the eighth embodiment device. Therefore, additional explanation on the constitution of the eighth embodiment device will be omitted.

[0070]

The manufacturing method of the eighth embodiment

device is the same as the manufacturing method of the seventh embodiment device except a point that the screen printing method is used for forming the conductor protective layer 5 in stead of the mask printing method, so that the explanation of the manufacturing method of the eighth embodiment device will be also omitted.

[0071]

The eighth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0072]

Fig. 9 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the ninth embodiment of the present invention. Also, Fig. 38 is a view showing a semiconductor device according to a ninth embodiment

of this invention and illustrates the structure of its substantial part. Further, Fig. 9 shows a sectional view taken along lines A-B in Fig. 38.

[0073]

In Fig. 9 and Fig. 38, the same numeral is assigned to each of the same components as those shown in Fig. 7.

[0074]

The constituent difference between the aforementioned semiconductor device of the seventh embodiment (hereinafter, referred to as the seventh embodiment device again) and the semiconductor device of the ninth embodiment (hereinafter, referred to as the ninth embodiment device) is only a point that with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5, the seventh embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5 are installed on the same plane, while the ninth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside compared with the end (end face) of the stress cushioning layer 3 and the conductor protective

layer 5 of the outside part reaches the end surface 1(1) and there are no other constituent differences between the seventh embodiment device and the ninth embodiment device. Therefore, additional explanation on the constitution of the ninth embodiment device will be omitted.

[0075]

The manufacturing method of the ninth embodiment device is the same as the manufacturing method of the seventh embodiment device, so that the explanation on the manufacturing method of the ninth embodiment device will be also omitted.

[0076]

The ninth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0077]

Fig. 10 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the tenth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a tenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 10 shows a sectional view taken along lines A-B in Fig. 40.

[0078]

In the following explanation, the semiconductor device of the tenth embodiment is referred to as the tenth embodiment device.

[0079]

In Fig. 10 and Fig. 40, numeral 7 indicates a semiconductor element protective layer, and 7(1) indicates an opening (first opening) formed in the semiconductor element protective layer 7, and the same numeral is assigned to each of the same components as those shown in Fig. 1. In the following explanation, the opening 3(1) formed in the stress cushioning layer 3 in correspondence with the first opening 7(1) is assumed as a second opening.

[0080]

The semiconductor element protective layer 7 is formed on one side of the semiconductor element 1

where the electrode pad 2 and an integrated circuit portion not shown in the drawing are formed and arranged, and the first opening 7(1) is installed on the electrode pad 2, and a slit portion reaching the bottom of the semiconductor element protective layer 7 is installed on the end surface 1(1) of the semiconductor element 1. The stress cushioning layer 3 is formed on the semiconductor element protective layer 7, and the second opening 3(1) is installed in the position corresponding to the first opening 7(1) on the electrode pad 2, and a slit portion reaching the bottom of the stress cushioning layer 3 is installed on the end surface 1(1). The lead wire portion 4 is formed within the range from the electrode pad 2 to a part of the stress cushioning layer 3 via the first opening 7(1) and the second opening 3(1). The conductor protective layer 5 is formed on the stress cushioning layer 3 including the lead wire portion, and a plurality of window 5(1) are formed in a part of the lead wire portion 4, and a slit portion reaching the bottom of the conductor protective layer 5 is formed on the end surface 1(1). The external electrodes 6 are formed and arranged on the lead wire portion 4 via the windows 5(1).

[0081]

In this case, the end face of the semiconductor element protective layer 7 obtained by forming of the slit portion, the end face of the stress cushioning layer 3 obtained by forming of the slit portion, and the end face of the conductor protective layer 5 obtained by forming of the slit portion are positioned on the same plane respectively and the exposed end surface 1(1) is formed within the range from the end face of the semiconductor element 1 to the end face of the semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor protective layer 5 which are positioned on the same plane. The end face of the semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor protective layer 5 which are positioned on the same plane are positioned slightly inside a cutting scribe line formed on a semiconductor wafer.

[0082]

The manufacturing method of the semiconductor device of the tenth embodiment will be described hereunder.

[0083]

Firstly, positioning marks of aluminum (Al) indicating the intersection of scribe lines are formed

on one side of a semiconductor wafer of silicon (Si) or others, and the electrode pads 2 of aluminum (Al) are formed respectively in the areas enclosed by the positioning marks, and an integrated circuit portion (not shown in the drawing) is formed and arranged.

[0084]

Next, on the one side of the semiconductor wafer on which the positioning marks and the electrode pads 2 are formed, negative photosensitive polyimide resin is coated by spin coating and the semiconductor wafer is dried on a hot plate at 75°C for 105 seconds and then at 90°C for 105 seconds, then exposed using a predetermined mask, and heated again on the hot plate at 125°C for 60 seconds, and then developed. Thereafter, the semiconductor wafer is heated and cured in a nitrogen ($N_2$) atmosphere at 350°C for 60 seconds and the semiconductor element protective layer 7 having the opening 7(1) on the electrode pad 2 and the slit portion that the end surface 1(1) of the semiconductor wafer 1 is exposed linearly as far as about 100 μm inside the end face of the semiconductor element 1 is formed.

[0085]

Next, the aluminum (Al) oxide film is removed from the surface of the electrode pad 2 by sputter etching

using argon (Ar) gas.

[0086]

The forming process of the stress cushioning layer 3 to be installed on the semiconductor element protective layer 7 thereafter, the forming process of the lead wire portion 4 reaching a part of the stress cushioning layer 3 from the electrode pad 2 via the first opening 7(1) and the second opening 3(1), the forming process of the conductor protective layer 5 to be installed on the stress cushioning layer 3 including the lead wire portion 4, the forming process of the external electrodes 6 to be formed on the lead wire portion 4, and the cutting process of a semiconductor wafer are the same as the corresponding respective forming processes of the manufacturing method of the first embodiment device, so that additional explanation on the manufacturing method of the tenth semiconductor device will be omitted.

[0087]

The tenth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is

found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0088]

Fig. 11 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the eleventh embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to an eleventh embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 11 shows a sectional view taken along lines A-B in Fig. 41.

[0089]

In Fig. 11 and Fig. 41, the same numeral is assigned to each of the same components as those shown in Figs. 1 and 2.

[0090]

The constituent difference between the aforementioned semiconductor device of the tenth embodiment (hereinafter, referred to as the tenth embodiment device again) and the semiconductor device of the eleventh embodiment (hereinafter, referred to

as the eleventh embodiment device) is only a point that with respect to the constitution of the slit portions of the semiconductor element protective layer 7 and the stress cushioning layer 3 and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the tenth embodiment device is structured so that the end face of the semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor protective layer 5 are installed on the same plane, while the eleventh embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the stress cushioning layer 3 are positioned on the same plane and the end face of the conductor protective layer 5 is positioned on the inside compared with the same plane and the exposed end surface 3(2) is installed on the stress cushioning layer 3 and there are no other constituent differences between the tenth embodiment device and the eleventh embodiment device. Therefore, additional explanation on the constitution of the eleventh embodiment device will be omitted.

[0091]

The manufacturing method of the eleventh

embodiment device is the same as the manufacturing method of the tenth embodiment device, so that the explanation on the manufacturing method of the tenth embodiment device will be omitted.

[0092]

The eleventh embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0093]

Fig. 12 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twelfth embodiment of the present invention. Also, Fig. 42 is a view showing a semiconductor device according to a twelfth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 12 shows a sectional view taken along lines A-B in Fig. 42.

[0094]

In Fig. 12 and Fig. 42, numeral 7(2) indicates the exposed end surface of the semiconductor element protective layer 7 and the same numeral is assigned to each of the same components as those shown in Fig. 11.

[0095]

The constituent difference between the aforementioned semiconductor device of the eleventh embodiment (hereinafter, referred to as the first embodiment device again) and the semiconductor device of the twelfth embodiment (hereinafter, referred to as the twelfth embodiment device) is only a point that with respect to the constitution of the slip portion of the semiconductor element protective layer 7 and the slit portion of the stress cushioning layer 3 on the end surface 1(1) of the semiconductor element 1, the eleventh embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the stress cushioning layer 3 are installed on the same plane, while the twelfth embodiment device is structured so that the end face of the stress cushioning layer 3 is positioned on the inside compared with the end face of the semiconductor element protective layer 7 and the exposed end surface 7(2) is installed on the

semiconductor element protective layer 7 and there are no other constituent differences between the eleventh embodiment device and the twelfth embodiment device. Therefore, additional explanation on the constitution of the twelfth embodiment device will be omitted.

[0096]

The manufacturing method of the twelfth embodiment device is the same as the manufacturing method of the eleventh embodiment device, so that the explanation on the manufacturing method of the twelfth embodiment device will be omitted.

[0097]

The twelfth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0098]

Fig. 13 is a cross sectional view showing the

constitution of the essential section of the semiconductor device of the thirteenth embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to a thirteenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 13 shows a sectional view taken along lines A-B in Fig. 41.

[0099]

In Fig. 13 and Fig. 41, the same numeral is assigned to each of the same components as those shown in Fig. 11.

[0100]

The constituent difference between the aforementioned semiconductor device of the eleventh embodiment (hereinafter, referred to as the eleventh embodiment device again) and the semiconductor device of the thirteenth embodiment (hereinafter, referred to as the thirteenth embodiment device) is only a point that with respect to the constitution of the slip portion of the semiconductor element protective layer 7 and the slit portion of the stress cushioning layer 3 on the end surface 1(1) of the semiconductor element 1, the eleventh embodiment device is structured so that the end face of the semiconductor element

protective layer 7 and the end face of the stress cushioning layer 3 are installed on the same plane, while the thirteenth embodiment device is structured so that the end face of the stress cushioning layer 3 is positioned on the outside compared with the end face of the semiconductor element protective layer 7 and the stress cushioning layer 3 of the outside part reaches the end surface 1(1) and there are no other constituent differences between the eleventh embodiment device and the thirteenth embodiment device. Therefore, additional explanation on the constitution of the thirteenth embodiment device will be omitted.

[0101]

The manufacturing method of the thirteenth embodiment device is the same as the manufacturing method of the eleventh embodiment device, so that the explanation on the manufacturing method of the thirteenth embodiment device will be omitted.

[0102]

The thirteenth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately

after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0103]

Fig. 14 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the fourteenth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a fourteenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 14 shows a sectional view taken along lines A-B in Fig. 40.

[0104]

In Fig. 14 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 11.

[0105]

The constituent difference between the aforementioned semiconductor device of the eleventh embodiment (hereinafter, referred to as the eleventh embodiment device again) and the semiconductor device of the fourteenth embodiment (hereinafter, referred to

as the fourteenth embodiment device) is only a point that with respect to the constitution of the slit portion of the stress cushioning layer 3 , the slit portion of the semiconductor element protective layer 7, and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the eleventh embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the stress cushioning layer 3 are installed on the same plane and the end face of the conductor protective layer 5 is positioned on the inside compared with this same plane, while the fourteenth embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the stress cushioning layer 3 are installed on the same plane and the end face of the conductor protective layer 5 is positioned on the outside compared with this same plane and the conductor protective layer 5 of the outside part reaches the end surface 1(1) and there are no other constituent differences between the eleventh embodiment device and the fourteenth embodiment device. Therefore, additional explanation on the constitution of the fourteenth embodiment device will be omitted.

[0106]

The manufacturing method of the fourteenth embodiment device is the same as the manufacturing method of the eleventh embodiment device, so that the explanation on the manufacturing method of the fourteenth embodiment device will be omitted.

[0107]

The fourteenth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0108]

Fig. 15 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the fifteenth embodiment of the present invention. Also, Fig. 43 is a view showing a semiconductor device according to a fifteenth embodiment of this invention and illustrates the

structure of its substantial part. Further, Fig. 15 shows a sectional view taken along lines A-B in Fig. 43.

[0109]

In Fig. 15 and Fig. 43, the same numeral is assigned to each of the same components as those shown in Fig. 12.

[0110]

The constituent difference between the aforementioned semiconductor device of the twelfth embodiment (hereinafter, referred to as the twelfth embodiment device again) and the semiconductor device of the fifteenth embodiment (hereinafter, referred to as the fifteenth embodiment device) is only a point that with respect to the constitution of the slit portion of the stress cushioning layer 3 and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the twelfth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the inside compared with the end face of the stress cushioning layer 3, while the fifteenth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside compared with the end face of the stress

cushioning layer 3 and the conductor protective layer 5 of the outside part reaches the exposed end surface 7(2) of the semiconductor element protective layer 7 and there are no other constituent differences between the twelfth embodiment device and the fifteenth embodiment device. Therefore, additional explanation on the constitution of the fifteenth embodiment device will be omitted.

[0111]

The manufacturing method of the fifteenth embodiment device is the same as the manufacturing method of the twelfth embodiment device, so that the explanation on the manufacturing method of the fifteenth embodiment device will be omitted.

[0112]

The fifteenth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that

there are no defective samples at all.

[0113]

Fig. 16 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the sixteenth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a sixteenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 16 shows a sectional view taken along lines A-B in Fig. 40.

[0114]

In Fig. 16 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 12.

[0115]

The constituent difference between the aforementioned semiconductor device of the twelfth embodiment (hereinafter, referred to as the twelfth embodiment device again) and the semiconductor device of the sixteenth embodiment (hereinafter, referred to as the sixteenth embodiment device) is only a point that with respect to the constitution of the slit portion of the semiconductor element protective layer 7, the slit portion of the stress cushioning layer 3,

and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the twelfth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the inside compared with the end face of the stress cushioning layer 3, while the sixteenth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside as compared with the end face of the stress cushioning layer 3 and the end face of the semiconductor element protective layer 7 and the conductor protective layer 5 of the outside part reaches the exposed end surface 7(2) of the semiconductor element protective layer 7 and the end surface 1(1) of the semiconductor element 1 and there are no other constituent differences between the twelfth embodiment device and the sixteenth embodiment device. Therefore, additional explanation on the constitution of the sixteenth embodiment device will be omitted.

[0116]

The manufacturing method of the sixteenth embodiment device is the same as the manufacturing method of the twelfth embodiment device, so that the explanation on the manufacturing method of the

sixteenth embodiment device will be omitted.

[0117]

The sixteenth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0118]

Fig. 17 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the seventeenth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a seventeenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 17 shows a sectional view taken along lines A-B in Fig. 40.

[0119]

In Fig. 17 and Fig. 40, the same numeral is

assigned to each of the same components as those shown in Fig. 13.

[0120]

The constituent difference between the aforementioned semiconductor device of the thirteenth embodiment (hereinafter, referred to as the thirteenth embodiment device again) and the semiconductor device of the seventeenth embodiment (hereinafter, referred to as the seventeenth embodiment device) is only a point that with respect to the constitution of the slit portion of the stress cushioning layer 3 and the slit portion of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1, the thirteenth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the inside compared with the end face of the stress cushioning layer 3, while the seventeenth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside compared with the end face of the stress cushioning layer 3 and the conductor protective layer 5 of the outside part reaches the end surface 1(1) of the semiconductor element 1 and there are no other constituent differences between the thirteenth embodiment device and the seventeenth embodiment

device. Therefore, additional explanation on the constitution of the seventeenth embodiment device will be omitted.

[0121]

The manufacturing method of the seventeenth embodiment device is the same as the manufacturing method of the thirteenth embodiment device, so that the explanation on the manufacturing method of the seventeenth embodiment device will be omitted.

[0122]

The seventeenth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0123]

Fig. 18 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the eighteenth embodiment of

the present invention. Also, Fig. 40 is a view showing a semiconductor device according to an eighteenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 18 shows a sectional view taken along lines A-B in Fig. 40.

[0124]

In Fig. 18 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 10.

[0125]

The constituent difference between the aforementioned semiconductor device of the tenth embodiment (hereinafter, referred to as the tenth embodiment device again) and the semiconductor device of the eighteenth embodiment (hereinafter, referred to as the eighteenth embodiment device) is only a point that with respect to the constitution of the end area of the stress cushioning layer 3 and the end area of the conductor protective layer 5, the tenth embodiment device is structured so that a slit portion is formed in the stress cushioning layer 3, and a slit portion is also formed in the conductor protective layer 5, and their end faces are installed on the same plane, while the eighteenth embodiment device is structured

so that a tapered portion becoming thinner taperingly toward the end face is formed on the stress cushioning layer 3, and a slit portion is formed in the conductor protective layer 5, and the end (end face) of the tapered portion and the end face of the slit portion are installed on the same plane, and the thickness of the conductor protective layer 5 replenishes to changes in the thickness of the tapered portion and there are no other constituent differences between the tenth embodiment device and the eighteenth embodiment device. Therefore, additional explanation on the constitution of the eighteenth embodiment device will be omitted.

[0126]

As compared with the manufacturing method of the tenth embodiment device, the manufacturing method of the eighteenth embodiment device has only a difference that with respect to the forming means of the stress cushioning layer 3, the manufacturing method of the tenth embodiment device forms the stress cushioning layer 3 including the opening 3(1) having a gently-inclined rising portion using the mask printing method and then forms a slit portion in the stress cushioning layer 3 by laser processing, while the manufacturing method of the eighteenth embodiment device forms the

stress cushioning layer 3 including the opening 3(1) having a gently-inclined rising portion and a tapered portion becoming thinner taperingly toward the end face using the mask printing method and does not perform the subsequent laser processing for the stress cushioning layer 3 and there are no other differences between the manufacturing method of the tenth embodiment device and the manufacturing method of the eighteenth embodiment device. Therefore, additional explanation on the manufacturing method of the eighteenth embodiment device will be omitted.

[0127]

The eighteenth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0128]

Fig. 19 is a cross sectional view showing the

constitution of the essential section of the semiconductor device of the nineteenth embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to a nineteenth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 19 shows a sectional view taken along lines A-B in Fig. 41.

[0129]

In Fig. 19 and Fig. 41, the same numeral is assigned to each of the same components as those shown in Figs. 5 and 18.

[0130]

The constituent difference between the aforementioned semiconductor device of the eighteenth embodiment (hereinafter, referred to as the eighteenth embodiment device again) and the semiconductor device of the nineteenth embodiment (hereinafter, referred to as the nineteenth embodiment device) is only a point that with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5, the eighteenth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are

installed on the same plane, while the nineteenth embodiment device is structured so that the end (end face) of the conductor protective layer 5 is positioned on the inside compared with the end (end face) of the stress cushioning layer 3 and the exposed end surface 3(2) is installed on the stress cushioning layer 3 and there are no other constituent differences between the eighteenth embodiment device and the nineteenth embodiment device. Therefore, additional explanation on the constitution of the nineteenth embodiment device will be omitted.

[0131]

The manufacturing method of the nineteenth embodiment device is the same as the manufacturing method of the eighteenth embodiment device except a point that the mask printing method is used for forming the conductor protective layer 5 in stead of the screen printing method, so that the explanation of the manufacturing method of the nineteenth embodiment device will be also omitted.

[0132]

The nineteenth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire

portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0133]

Fig. 20 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twentieth embodiment of the present invention. Also, Fig. 42 is a view showing a semiconductor device according to a twentieth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 20 shows a sectional view taken along lines A-B in Fig. 42.

[0134]

In Fig. 20 and Fig. 42, the same numeral is assigned to each of the same components as those shown in Figs. 12 and 19.

[0135]

The constituent difference between the aforementioned semiconductor device of the nineteenth embodiment (hereinafter, referred to as the nineteenth

embodiment device again) and the semiconductor device of the twentieth embodiment (hereinafter, referred to as the twentieth embodiment device) is only a point that with respect to the constitution of the end (end face) of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3, the nineteenth embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are installed on the same plane, while the twentieth embodiment device is structured so that the end face of the semiconductor element protective layer 7 is positioned on the outside compared with the end (end face) of the stress cushioning layer 3 and the exposed end surface 7(2) is installed on the semiconductor element protective layer 7 and there are no other constituent differences between the nineteenth embodiment device and the twentieth embodiment device. Therefore, additional explanation on the constitution of the twentieth embodiment device will be omitted.

[0136]

The manufacturing method of the twentieth embodiment device is the same as the manufacturing method of the nineteenth embodiment device except a

point that the screen printing method is used for forming the conductor protective layer 5 in stead of the mask printing method, so that the explanation of the manufacturing method of the twentieth embodiment device will be also omitted.

[0137]

The twentieth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0138]

Fig. 21 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-first embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to a twenty-first embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 21

shows a sectional view taken along lines A-B in Fig. 41.

[0139]

In Fig. 21 and Fig. 41, the same numeral is assigned to each of the same components as those shown in Fig. 19.

[0140]

The constituent difference between the aforementioned semiconductor device of the nineteenth embodiment (hereinafter, referred to as the nineteenth embodiment device again) and the semiconductor device of the twenty-first embodiment (hereinafter, referred to as the twenty-first embodiment device) is only a point that with respect to the constitution of the end (end face) of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3, the nineteenth embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are installed on the same plane, while the twenty-first embodiment device is structured so that the end face of the semiconductor element protective layer 7 is positioned on the inside compared with the end (end face) of the stress cushioning layer 3 and practically

installed on the same plane as that of the end face of the conductor protective layer 5 and there are no other constituent differences between the nineteenth embodiment device and the twenty-first embodiment device. Therefore, additional explanation on the constitution of the twenty-first embodiment device will be omitted.

[0141]

The manufacturing method of the twenty-first embodiment device is the same as the manufacturing method of the nineteenth embodiment device, so that the explanation on the manufacturing method of the twenty-first embodiment device will be omitted.

[0142]

The twenty-first embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0143]

Fig. 22 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-second embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a twenty-second embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 22 shows a sectional view taken along lines A-B in Fig. 40.

[0144]

In Fig. 22 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 18.

[0145]

The constituent difference between the aforementioned semiconductor device of the eighteenth embodiment (hereinafter, referred to as the eighteenth embodiment device again) and the semiconductor device of the twenty-second embodiment (hereinafter, referred to as the twenty-second embodiment device) is only a point that with respect to the constitution of the end area of the conductor protective layer 5, the eighteenth embodiment device is structured so that a slit portion is formed in the conductor protective

layer 5 and the end face of the conductor protective layer 5 is almost perpendicular to the end surface 1(1), while the twenty-second embodiment device is structured so that an inclined surface becoming thinner linearly toward the end face of the conductor protective layer 5 is formed and there are no other constituent differences between the eighteenth embodiment device and the twenty-second embodiment device. Therefore, additional explanation on the constitution of the twenty-second embodiment device will be omitted.

[0146]

When the manufacturing method of the twenty-second embodiment device is compared with the manufacturing method of the eighteenth embodiment device, the difference is only a point that with respect to the forming means of the conductor protective player 5, the manufacturing method of the eighteenth embodiment device forms the conductor protective layer 5 including the opening 3(1) having a gently-inclined rising portion and a slit portion having an end face almost perpendicular to the end surface 1(1) using the screen printing method, while the manufacturing method of the twenty-second embodiment device forms the conductor protective layer 5 including the opening

3(1) having a gently-inclined rising portion and an inclined surface having a linearly-inclined rising portion using the screen printing method and there are no other differences between the manufacturing method of the eighteenth embodiment device and the manufacturing method of the twenty-second embodiment device. Therefore, additional explanation on the manufacturing method of the twenty-second embodiment device will be omitted.

[0147]

The twenty-second embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0148]

Fig. 23 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-third embodiment of

the present invention: Also, Fig. 41 is a view showing a semiconductor device according to a twenty-third embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 23 shows a sectional view taken along lines A-B in Fig. 41.

[0149]

In Fig. 23 and Fig. 41, the same numeral is assigned to each of the same components as those shown in Figs. 5 and 22.

[0150]

The constituent difference between the aforementioned semiconductor device of the twenty-second embodiment (hereinafter, referred to as the twenty-second embodiment device again) and the semiconductor device of the twenty-third embodiment (hereinafter, referred to as the twenty-third embodiment device) is only a point that with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5, the twenty-second embodiment device is structured so that the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5 are installed on the same plane, while the twenty-third

embodiment device is structured so that the end (end face) of the conductor protective layer 5 is positioned on the inside compared with the end (end face) of the stress cushioning layer 3 and the exposed end surface 3(2) is installed on the stress cushioning layer 3 and there are no other constituent differences between the twenty-second embodiment device and the twenty-third embodiment device. Therefore, additional explanation on the constitution of the twenty-third embodiment device will be omitted.

[0151]

The manufacturing method of the twenty-third embodiment device is the same as the manufacturing method of the twenty-second embodiment device except a point that the mask printing method is used for forming the conductor protective layer 5 in stead of the screen printing method, so that the explanation of the manufacturing method of the twenty-third embodiment device will be also omitted.

[0152]

The twenty-third embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When

the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0153]

Fig. 24 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-fourth embodiment of the present invention. Also, Fig. 42 is a view showing a semiconductor device according to a twenty-fourth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 24 shows a sectional view taken along lines A-B in Fig. 42.

[0154]

In Fig. 24 and Fig. 42, the same numeral is assigned to each of the same components as those shown in Figs. 20 and 23.

[0155]

The constituent difference between the aforementioned semiconductor device of the twenty-third embodiment (hereinafter, referred to as the twenty-third embodiment device again) and the

semiconductor device of the twenty-fourth embodiment (hereinafter, referred to as the twenty-fourth embodiment device) is only a point that with respect to the constitution of the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3, the twenty-third embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are installed on the same plane, while the twenty-fourth embodiment device is structured so that the end face of the semiconductor element protective layer 7 is positioned on the outside compared with the end (end face) of the stress cushioning layer 3 and the exposed end surface 7(2) is installed on the semiconductor element protective layer 7 and there are no other constituent differences between the twenty-third embodiment device and the twenty-fourth embodiment device. Therefore, additional explanation on the constitution of the twenty-fourth embodiment device will be omitted.

[0156]

The manufacturing method of the twenty-fourth embodiment device is the same as the manufacturing method of the twenty-third embodiment device except a

point that the screen printing method is used for forming the conductor protective layer 5 in stead of the mask printing method, so that the explanation of the manufacturing method of the twenty-fourth embodiment device will be also omitted.

[0157]

The twenty-fourth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0158]

Fig. 25 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-fifth embodiment of the present invention. Also, Fig. 41 is a view showing a semiconductor device according to a twenty-fifth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 25

shows a sectional view taken along lines A-B in Fig. 41.

[0159]

In Fig. 25 and Fig. 41, the same numeral is assigned to each of the same components as those shown in Fig. 23.

[0160]

The constituent difference between the aforementioned semiconductor device of the twenty-third embodiment (hereinafter, referred to as the twenty-third embodiment device again) and the semiconductor device of the twenty-fifth embodiment (hereinafter, referred to as the twenty-fifth embodiment device) is only a point that with respect to the constitution of the end (end face) of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3, the twenty-third embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are installed on the same plane, while the twenty-fifth embodiment device is structured so that the end face of the semiconductor element protective layer 7 is positioned on the inside compared with the end (end face) of the stress

cushioning layer 3 and practically installed on the same plane as that of the end (end face) of the conductor protective layer 5 and there are no other constituent differences between the twenty-third embodiment device and the twenty-fifth embodiment device. Therefore, additional explanation on the constitution of the twenty-fifth embodiment device will be omitted.

[0161]

The manufacturing method of the twenty-fifth embodiment device is the same as the manufacturing method of the twenty-third embodiment device, so that the explanation on the manufacturing method of the twenty-fifth embodiment device will be also omitted.

[0162]

The twenty-fifth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that

there are no defective samples at all.

[0163]

Fig. 26 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-sixth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a twenty-sixth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 26 shows a sectional view taken along lines A-B in Fig. 40.

[0164]

In Fig. 26 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 18.

[0165]

The constituent difference between the aforementioned semiconductor device of the eighteenth embodiment (hereinafter, referred to as the eighteenth embodiment device again) and the semiconductor device of the twenty-sixth embodiment (hereinafter, referred to as the twenty-sixth embodiment device) is only a point that with respect to the constitution of the end face of the semiconductor element protective layer 7, the end (end face) of the stress cushioning layer 3,

and the end face of the conductor protective layer 5, the eighteenth embodiment device is structured so that the end face of the semiconductor element protective layer 7, the end (end face) of the stress cushioning layer 3, and the end face of the conductor protective layer 5 are installed on the same plane, while the twenty-sixth embodiment device is structured so that although the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are positioned on the same plane, the end face of the semiconductor element protective layer 7 is positioned on the outside compared with the same plane, and the semiconductor element protective layer 7 of the outside part reaches the end surface 1(1) of the semiconductor element 1, and there are no other constituent differences between the eighteenth embodiment device and the twenty-sixth embodiment device. Therefore, additional explanation on the constitution of the twenty-sixth embodiment device will be omitted.

[0166]

The manufacturing method of the twenty-sixth embodiment device is the same as the manufacturing method of the eighteenth embodiment device, so that the explanation on the manufacturing method of the

twenty-sixth embodiment device will be also omitted.

[0167]

The twenty-sixth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0168]

Fig. 27 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-seventh embodiment of the present invention. Also, Fig. 43 is a view showing a semiconductor device according to a twenty-seventh embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 27 shows a sectional view taken along lines A-B in Fig. 43.

[0169]

In Fig. 27 and Fig. 43, the same numeral is

assigned to each of the same components as those shown in Fig. 20.

[0170]

The constituent difference between the aforementioned semiconductor device of the twentieth embodiment (hereinafter, referred to as the twentieth embodiment device again) and the semiconductor device of the twenty-seventh embodiment (hereinafter, referred to as the twenty-seventh embodiment device) is only a point that with respect to the constitution of the end face of the conductor protective layer 5, the twentieth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the inside compared with the end face of the stress cushioning layer 3, while the twenty-seventh embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside compared with the end face of the stress cushioning layer 3 and the conductor protective layer 5 of the outside part reaches the exposed end surface 7(2) of the semiconductor element protective layer 7 and there are no other constituent differences between the twentieth embodiment device and the twenty-seventh embodiment device. Therefore, additional explanation on the constitution of the

twenty-seventh embodiment device will be omitted.

[0171]

The manufacturing method of the twenty-seventh embodiment device is the same as the manufacturing method of the twentieth embodiment device except a point that the mask printing method is used for forming the conductor protective layer 5 in stead of the screen printing method, so that the explanation of the manufacturing method of the twenty-seventh embodiment device will be also omitted.

[0172]

The twenty-seventh embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0173]

Fig. 28 is a cross sectional view showing the constitution of the essential section of the

semiconductor device of the twenty-eighth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a twenty-eighth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 28 shows a sectional view taken along lines A-B in Fig. 40.

[0174]

In Fig. 28 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 27.

[0175]

The constituent difference between the aforementioned semiconductor device of the twenty-seventh embodiment (hereinafter, referred to as the twenty-seventh embodiment device again) and the semiconductor device of the twenty-eighth embodiment (hereinafter, referred to as the twenty-eighth embodiment device) is only a point that with respect to the constitution of the end face of the conductor protective layer 5, the twenty-seventh embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the inside compared with the end face of semiconductor element protective layer 7 and on the outside compared

with the end (end face) of the stress cushioning layer 3, while the twenty-eighth embodiment device is structured so that the end face of the conductor protective layer 5 is positioned on the outside compared with the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 and there are no other constituent differences between the twenty-seventh embodiment device and the twenty-eighth embodiment device. Therefore, additional explanation on the constitution of the twenty-eighth embodiment device will be omitted.

[0176]

The manufacturing method of the twenty-eighth embodiment device is the same as the manufacturing method of the twenty-seventh embodiment device except a point that the screen printing method is used for forming the conductor protective layer 5 in stead of the mask printing method, so that the explanation of the manufacturing method of the twenty-eighth embodiment device will be also omitted.

[0177]

The twenty-eighth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4

and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0178]

Fig. 29 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the twenty-ninth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a twenty-ninth embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 29 shows a sectional view taken along lines A-B in Fig. 40.

_[0179]

In Fig. 29 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 28.

[0180]

The constituent difference between the aforementioned semiconductor device of the twenty-

eighth embodiment (hereinafter, referred to as the twenty-eighth embodiment device again) and the semiconductor device of the twenty-ninth embodiment (hereinafter, referred to as the twenty-ninth embodiment device) is only a point that with respect to the constitution of the end face of the conductor protective layer 5 and the end (end face) of the stress cushioning layer 3, the twenty-eighth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 is positioned on the inside compared with the end face of the semiconductor element protective layer 7, while the twenty-ninth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 is positioned on the outside compared with the end face of the semiconductor element layer 7 and the end (end face) of the stress cushioning layer 3 of the outside part reaches the surface of the semiconductor element 1 and there are no other constituent differences between the twenty-eighth embodiment device and the twenty-ninth embodiment device. Therefore, additional explanation on the constitution of the twenty-ninth embodiment device will be omitted.

[0181]

The manufacturing method of the twenty-ninth

embodiment device is the same as the manufacturing method of the twenty-eighth embodiment device except a point that the mask printing method is used for forming the conductor protective layer 5 in stead of the screen printing method, so that the explanation of the manufacturing method of the twenty-ninth embodiment device will be also omitted.

[0182]

The twenty-ninth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0183]

Fig. 30 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the thirtieth embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a thirtieth

embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 30 shows a sectional view taken along lines A-B in Fig. 40.

[0184]

In Fig. 30 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 22.

[0185]

The constituent difference between the aforementioned semiconductor device of the twenty-second embodiment (hereinafter, referred to as the twenty-second embodiment device again) and the semiconductor device of the thirtieth embodiment (hereinafter, referred to as the thirtieth embodiment device) is only a point that with respect to the constitution of the end face of the conductor protective layer 5, the twenty-second embodiment device is structured so that the end face of the semiconductor element protective layer 7, the end (end face) of the stress cushioning layer 3, and the end (end face) of the conductor protective layer 5 are respectively installed on the same plane, while the thirtieth embodiment device is structured so that the end face of the semiconductor element protective layer

7 and the end (end face) of the stress cushioning layer 3 are installed on the same plane, and the end (end face) of the conductor protective layer 5 is positioned on the outside compared with this same plane, and the end (end face) of the conductor protective layer 5 of the outside part reaches the surface of the semiconductor element 1 and there are no other constituent differences between the twenty-second embodiment device and the thirtieth embodiment device. Therefore, additional explanation on the constitution of the thirtieth embodiment device will be omitted.

[0186]

The manufacturing method of the thirtieth embodiment device is the same as the manufacturing method of the twenty-second embodiment device, so that the explanation on the manufacturing method of the thirtieth embodiment device will be also omitted.

[0187]

The thirtieth embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately

after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0188]

Fig. 31 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the thirty-first embodiment of the present invention. Also, Fig. 42 is a view showing a semiconductor device according to a thirty-first embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 31 shows a sectional view taken along lines A-B in Fig. 42.

[0189]

In Fig. 31 and Fig. 42, the same numeral is assigned to each of the same components as those shown in Fig. 24.

[0190]

The constituent difference between the aforementioned semiconductor device of the twenty-fourth embodiment (hereinafter, referred to as the twenty-fourth embodiment device again) and the semiconductor device of the thirty-first embodiment

(hereinafter, referred to as the thirty-first embodiment device) is only a point that with respect to the constitution of the end (end face) of the stress cushioning layer 3 and the end (end face) of the conductor protective layer 5, the twenty-fourth embodiment device is structured so that the end (end face) of the stress cushioning layer 3 is positioned on the outside compared with the end (end face) of the conductor protective layer 5 and the exposed end surface 3(2) is installed on the stress cushioning layer 3, while the thirty-first embodiment device is structured so that the end face of the semiconductor element protective layer 7 and the end (end face) of the stress cushioning layer 3 are installed on the same plane and the end (end face) of the stress cushioning layer 3 is positioned on the inside compared with the end (end face) of the conductor protective layer 5 and there are no other constituent differences between the twenty-fourth embodiment device and the thirty-first embodiment device. Therefore, additional explanation on the constitution of the thirty-first embodiment device will be omitted.

[0191]

The manufacturing method of the thirty-first embodiment device is the same as the manufacturing

method of the twenty-fourth embodiment device except a point that the mask printing method is used for forming the conductor protective layer 5 in stead of the screen printing method, so that the explanation of the manufacturing method of the thirty-first embodiment device will be also omitted.

[0192]

The thirty-first embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0193]

Fig. 32 is a cross sectional view showing the constitution of the essential section of the semiconductor device of the thirty-second embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a thirty-second embodiment of this invention and illustrates

the structure of its substantial part. Further, Fig. 32 shows a sectional view taken along lines A-B in Fig. 40.

[0194]

In Fig. 32 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 28.

[0195]

The constituent difference between the aforementioned semiconductor device of the twenty-eighth embodiment (hereinafter, referred to as the twenty-eighth embodiment device again) and the semiconductor device of the thirty-second embodiment (hereinafter, referred to as the thirty-second embodiment device) is only a point that with respect to the constitution of the end (end face) of the conductor protective layer 5, the twenty-eighth embodiment device is structured so that the end face of the conductor protective layer 5 is installed on the surface of the semiconductor element 1 in the standing state due to forming of the slit portion, while the thirty-second embodiment device is structured so that the end (end face) of the conductor protective layer 5 is formed as a plurality of inclined surfaces having a different inclination angle

stepwise and there are no other constituent differences between the twenty-eighth embodiment device and the thirty-second embodiment device. Therefore, additional explanation on the constitution of the thirty-second embodiment device will be omitted.

[0196]

The manufacturing method of the thirty-second embodiment device is the same as the manufacturing method of the twenty-eighth embodiment device, so that the explanation on the manufacturing method of the thirty-second embodiment device will be also omitted.

[0197]

The thirty-second embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0198]

Fig. 33 is a cross sectional view showing the

constitution of the essential section of the semiconductor device of the thirty-third embodiment of the present invention. Also, Fig. 40 is a view showing a semiconductor device according to a thirty-second embodiment of this invention and illustrates the structure of its substantial part. Further, Fig. 32 shows a sectional view taken along lines A-B in Fig. 40.

[0199]

In Fig. 33 and Fig. 40, the same numeral is assigned to each of the same components as those shown in Fig. 29.

[0200]

The constituent difference between the aforementioned semiconductor device of the twenty-ninth embodiment (hereinafter, referred to as the twenty-ninth embodiment device again) and the semiconductor device of the thirty-third embodiment (hereinafter, referred to as the thirty-third embodiment device) is only a point that with respect to the constitution of the end (end face) of the conductor protective layer 5, the twenty-ninth embodiment device is structured so that the end face of the conductor protective layer 5 is installed on the surface of the semiconductor element 1 in the

standing state due to forming of the slit portion, while the thirty-third embodiment device is structured so that the end (end face) of the conductor protective layer 5 is formed as a plurality of inclined surfaces having a different inclination angle stepwise and there are no other constituent differences between the twenty-ninth embodiment device and the thirty-third embodiment device. Therefore, additional explanation on the constitution of the thirty-third embodiment device will be omitted.

[0201]

The manufacturing method of the thirty-third embodiment device is the same as the manufacturing method of the twenty-ninth embodiment device, so that the explanation on the manufacturing method of the thirty-third embodiment device will be also omitted.

[0202]

The thirty-third embodiment device manufactured by such a method is evaluated on the suitability immediately after forming of the lead wire portion 4 and there are no unsuitable (defective) lead wire portions found at all in all the evaluated ones. When the appearance inspection is executed immediately after dicing, it is found that there are no defective semiconductor packages at all and when the same

temperature test as that performed for the first embodiment device is executed, it is also found that there are no defective samples at all.

[0203]

Meanwhile, with respect to the semiconductor element protective layer 7 to be used for the semiconductor devicees of the tenth to thirty-third embodiments, if a usable material can protect the semiconductor element 1 from an external environment, it is not limited to the aforementioned negative type photosensitive polyimide resin. Namely, the usable materials may be polyimide, polycarbonate, polyester, polytetrafluoroethylene, polyethylene, polypropylene, polyvinylidene fluoride, cellulose acetate, polysulfone, polyacrylonitrile, polyamide, polyamide-imide, epoxy, maleic-imide, phenol, cyanate, polyolefin, and polyurethane, compounds thereof, and mixtures of those compounds and rubber components such as acrylic rubber, silicone rubber, or nitrile-butadiene rubber, or organic compound filler such as polyimide filler, or inorganic filler such as silica. Furthermore, photosensitive materials including these materials may be used.

[0204]

With respect to the stress cushioning layer 3 to

be used for the semiconductor devicees of the first to thirty-third embodiments, a usable material is preferably a low-elastomeric resin because it must cushion stress. Concretely, the usable materials may be fluororubber, silicone rubber, silicone fluoride rubber, acrylic rubber, hydrogenated nitrile rubber, ethylene propylene rubber, chlorosulfonated polystyrene, epichlorohydrin rubber, butyl rubber, urethane rubber, polycarbonate/acrylonitrile butadiene styrene alloy, polysiloxane dimethyl terephthalate/polyethylene terephthalate copolymer polybutylene terephthalate/polycarbonate alloy, polytetrafluoroethylene, fluorinated ethylene propylene, polyarylate, polyamide/acrylonitrile butadiene styrene alloy, denatured epoxy, denatured polyolefin, and siloxane detnatured polyamide-imide. In addition to them, various kinds of thermoset resins, or materials combining two or more thermoset resins, or materials with inorganic fillers mixed in thermoset resins may be used such as epoxy resin, unsaturated polyester resin, epoxy isocyanate resin, maleic-imide resin, maleic-imide epoxy resin, cyanate ester resin, cyanate ester epoxy resin, cyanate ester maleic-imide resin, phenolic resin, diallyl phthalate resin, urethane resin, cyanamide resin, and maleic-imide

cyanamide resin. Further, photosensitivity is given to these resins and the form of the stress cushioning layer 3 can be controlled by a predetermined exposure-development process.

[0205]

In this case, with respect to the semiconductor device of the present invention, various kinds of semiconductor devicees are manufactured by changing the thickness of the stress cushioning layer 3 and the size of the semiconductor element 1, and each of the semiconductor devicees is mounted on a mounting substrate, and the mounting reliability evaluation test is executed within the temperature range from -55°C to 125°C. The result shows that assuming the thickness of the stress cushioning layer 3 as t and the distance from the center of gravity of the semiconductor element 1 to the outermost end of the semiconductor element 1 as R, when the relationship of t and R satisfies the formula $t/R \geq 0.01$. the mounting reliability is satisfactory.

[0206]

Furthermore, the lead wire portion 4 to be used for the semiconductor devicees of the first to thirty-third embodiments uses a material of gold (Au), copper (Cu), or aluminum (Al) or a material of copper (Cu) or

aluminum (Al) with its surface plated with gold (Au).

[0207]

The conductor protective layer 5 to be used for the semiconductor devicees of the first to thirty-third embodiments is not limited to the material to be used. However, an organic combined part such as epoxy resin, polyimide resin, or polyamide resin compounded with an inorganic filler is generally formed on the stress cushioning layer 3 including the lead wire portion 4 excluding the connected portion of the lead wire portion 4 and the external electrode 6 by screen printing. In this case, a material with photosensitivity given may be added.

[0208]

Furthermore, the external electrode 6 to be used for the semiconductor devicees of the first to thirty-third embodiments is a conductor electrically connected to the substrate with the semiconductor device mounted, so that the material to be used may be, concretely, a solder alloy including tin (Sn), zinc (Zn), or lead (Pb), or silver (Ag), Copper (Cu), or gold (Au), or a solder alloy, silver (Ag), or copper (Cu) which is covered with gold (Au) and formed in a ball shape. In addition to these materials, a metal such as molybdenum (Mo), nickel (Ni), copper (Cu),

platinum (Pt), or titanium (Ti), or an alloy composed of two or more kinds of the aforementioned metals, or a multi-layer composed of two or more layers may be used.

[0209]

Next, to compare differences in characteristics with the semiconductor devicees of the first to thirty-third embodiments, some semiconductor devicees are separately formed as comparison examples.

[0210]

Fig. 34 is a cross sectional view showing the constitution of the essential section of a semiconductor device as a first comparison example. Also, Fig. 44 is a view showing a semiconductor device which is a first comparison example and illustrates the structure of its substantial part. Further, Fig. 34 shows a sectional view taken along lines A-B in Fig. 44.

[0211]

In Fig. 34 and Fig. 44, the same numeral is assigned to each of the same components as those shown in Fig. 1.

[0212]

The constituent difference between the aforementioned semiconductor device of the first

embodiment (hereinafter, referred to as the first embodiment device again) and the semiconductor device of the first comparison example (hereinafter, referred to as the first comparison example device) is only a point that with respect to the constitution of the end areas of the stress cushioning layer 3 and the conductor protective layer 5, the first embodiment device is structured so that the stress cushioning layer 3 and the conductor protective layer 5 have slit portions reaching the bottom of the stress cushioning layer 3 and the bottom of the conductor protective layer 5 respectively, thereby the end face of the stress cushioning layer 3 and the end face of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1 are formed inside the cutting scribe line formed on a semiconductor wafer, and the end surface 1(1) of the semiconductor element 1 is exposed within the range from the end face to the inside of the scribe line, while the first comparison example device is structured so that the end face of the stress cushioning layer 3 and the end face of the conductor protective layer 5 are installed on the same plane as that of the end face of the semiconductor element 1 and the semiconductor element 1 has no exposed end surface 1(1) and there are no other

constituent differences between the first embodiment device and the first comparison example device. Therefore, additional explanation on the constitution of the first comparison example device will be omitted.

[0213]

The manufacturing method of this first comparison example device will be described hereunder. Firstly, positioning marks of aluminum (Al) indicating an intersection of scribe lines are formed on one side of a semiconductor wafer of silicon (Si) and in the areas enclosed by the positioning marks, the electrode pads 2 of aluminum (Al) are formed respectively and an integrated circuit portion (not shown in the drawing) is formed.

[0214]

Next, on one side of the semiconductor wafer with the positioning marks and electrode pads 2 formed, an uncured dry film composed of epoxy resin, orthocresol novolac curing agent, acrylic rubber, and silica filler which has a thickness of 100 μm and a coefficient of elasticity of 3000 MPa at room temperature after curing is adhered in an environment of 150°C using a roll laminator and the adhered dry film is heated and cured at 150°C for one hour, thus the stress cushioning layer 3 is formed.

[0215]

Next, the oxygen plasma etching is executed, and the residue of the stress cushioning layer 3 on the electrode pads 2 is removed, and the oxide film on the surface of the electrode pads 2 is also removed, and then a chromium (Cr) film with a thickness of 500 A is deposited in the opening 3(1) of the stress cushioning layer 3 and on the stress cushioning layer 3 respectively, and a copper (Cu) film with a thickness of 0.5 μm is deposited on it. Then, a negative type photosensitive resist is spin-coated on the deposited film and then prebaked, exposed, and developed and a resist wiring pattern with a thickness of 15 μm is formed. A copper (Cu) film with a thickness of 10 μm is formed inside the formed wiring pattern by electroplating and a nickel (Ni) film with a thickness of 2 μm is formed on it by electroplating. Thereafter, the resist is peeled off by a release liquid, and the copper (Cu) film in the deposited film is etched by an ammonium persulfate/sulfuric acid solution, and furthermore the chromium (Cr) film in the deposited film is etched by a potassium permanganate solution, and the lead wire portion 4 is formed. At the point of time when the lead wire portion 4 is formed, the same evaluation (the first

evaluation) as that for the semiconductor device of the first embodiment is performed.

[0216]

Then, photosensitive solder resist varnish is coated on the stress cushioning layer 3 including the lead wire portion 4 by screen printing, and the coated film is dried at 80°C for 20 minutes, then exposed and developed using a predetermined pattern, and heated and cured at 150°C for one hour, thereby the conductor protective layer 5 having a plurality of windows 5(1) at a part of the lead wire portion 4 is formed.

[0217]

Next, a gold (Au) deposit film with a thickness of 0.1 μm is formed on the nickel (Ni) film of the lead wire portion 4 which is exposed via the windows 5(1) by replacement plating. Thereafter, flux is coated on the gold (Au) deposit film using a metal mask, and solder balls of Sn-Ag-Cu series with a diameter of about 0.35 mm are put on it, and the solder balls are heated in an infrared reflow furnace at 260°C for 10 seconds, and the external electrodes 6 are formed.

[0218]

Finally, the semiconductor chip is cut with a dicing saw with a thickness of 0.2 mm along the scribe line and a plurality of semiconductor devicees are

obtained. In this case, the same evaluation (the second evaluation) as that for the semiconductor device of the first embodiment is performed for the obtained semiconductor devicees, and moreover the same temperature test as that for the semiconductor device of the first embodiment is executed, and then the evaluation (the third evaluation) is performed again.

[0219]

In the semiconductor devicees of the first comparison example manufactured by such a manufacturing method, at the first evaluation time, defective conductor patterns of about 30% are generated for the lead wire portion 4, and at the second evaluation (appearance inspection) time immediately after dicing, defective semiconductor devicees of about 20% are generated because large mechanical stress is applied to the cutting portion of a plurality of layers during dicing, and furthermore, at the third evaluation time after the temperature test, package defects such as a disconnection defect are generated in almost all samples because large mechanical stress during dicing and also large thermal stress during changing of the temperature are applied to the cutting portion of a plurality of layers.

[0220]

Fig. 35 is a cross sectional view showing the constitution of the essential section of a semiconductor device as a second comparison example. Also, Fig. 44 is a view showing a semiconductor device which is a second comparison example and illustrates the structure of its substantial part. Further, Fig. 35 shows a sectional view taken along lines A-B in Fig. 44.

[0221]

In Fig. 35 and Fig. 44, the same numeral is assigned to each of the same components as those shown in Fig. 6.

[0222]

The constituent difference between the aforementioned semiconductor device of the sixth embodiment (hereinafter, referred to as the sixth embodiment device again) and the semiconductor device of the second comparison example (hereinafter, referred to as the second comparison example device) is only a point that with respect to the constitution of the end area of the stress cushioning layer 3, the sixth embodiment device is structured so that the conductor protective layer 5 has a slit portion reaching the bottom thereof, thereby the end face of the conductor protective layer 5 on the end surface

1(1) of the semiconductor element 1 is formed inside the cutting scribe line formed on a semiconductor wafer, and the end surface 1(1) of the semiconductor element 1 is exposed within the range from the end face to the inside of the scribe line, while the second comparison example device is structured so that the end face of the conductor protective layer 5 is installed on the same plane as that of the end face of the semiconductor element 1 and the semiconductor element 1 has no exposed end surface 1(1) and there are no other constituent differences between the sixth embodiment device and the second comparison example device. Therefore, additional explanation on the constitution of the second comparison example device will be omitted.

[0223]

As compared with the manufacturing method of the sixth embodiment device, the manufacturing method of the second comparison example device has only a difference that the manufacturing method of the sixth embodiment device forms a slit portion in the conductor protective layer 5 when the conductor protective layer 5 is formed by screen printing, while the manufacturing method of the second comparison example device forms no slit in the conductor

protective layer 5 and there are no other differences between the manufacturing method of the sixth embodiment device and the manufacturing method of the second comparison example device. Therefore, additional explanation on the manufacturing method of the second comparison example device will be omitted.

[0224]

In the semiconductor devicees of the second comparison example manufactured by such a manufacturing method, at the first evaluation time, defective conductor patterns of 30% or more are generated for the lead wire portion 4, and at the second evaluation (appearance inspection) time immediately after dicing, defective semiconductor devices of about 20% are generated during dicing, and furthermore, at the third evaluation time after the temperature test, package defects such as a disconnection defect are generated in almost all samples.

[0225]

Fig. 36 is a cross sectional view showing the constitution of the essential section of a semiconductor device as a third comparison example. Also, Fig. 44 is a view showing a semiconductor device which is a third comparison example and illustrates

the structure of its substantial part. Further, Fig. 36 shows a sectional view taken along lines A-B in Fig. 44.

[0226]

In Fig. 36 and Fig. 44, the same numeral is assigned to each of the same components as those shown in Fig. 10.

[0227]

The constituent difference between the aforementioned semiconductor device of the tenth embodiment (hereinafter, referred to as the tenth embodiment device again) and the semiconductor device of the third comparison example (hereinafter, referred to as the third comparison example device) is only a point that with respect to the constitution of the respective end areas of the semiconductor element protective layer 7, the stress cushioning layer 3, and the conductor protective layer 5, the tenth embodiment device is structured so that the semiconductor element protective layer 7, the stress cushioning layer 3, and the conductor protective layer 5 respectively have slit portions reaching the bottom of the semiconductor element protective layer 7, the bottom of the stress cushioning layer 3, and the bottom of the conductor protective layer 5, thereby the end face of the

semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor protective layer 5 on the end surface 1(1) of the semiconductor element 1 are formed inside the cutting scribe line formed on a semiconductor wafer, and the end surface 1(1) of the semiconductor element 1 is exposed within the range from the end face to the inside of the scribe line, while the third comparison example device is structured so that the end face of the semiconductor element protective layer 7, the end face of the stress cushioning layer 3, and the end face of the conductor protective layer 5 are respectively installed on the same plane as that of the end face of the semiconductor element 1 and the semiconductor element 1 has no exposed end surface 1(1) and there are no other constituent differences between the tenth embodiment device and the third comparison example device. Therefore, additional explanation on the constitution of the third comparison example device will be omitted.

[0228]

The manufacturing method of the third comparison example device is the same as the manufacturing method of the tenth embodiment device, so that the explanation on the manufacturing method of the third

comparison example device will be omitted.

[0229]

In the semiconductor devicees of the third comparison example manufactured by such a manufacturing method, at the first evaluation time, defective conductor patterns of slightly lower than 30% are generated for the lead wire portion 4, and at the second evaluation (appearance inspection) time immediately after dicing, defective semiconductor devicees of about 30% are generated during dicing, and furthermore, at the third evaluation time after the temperature test, package defects such as a disconnection defect are generated in almost all samples.

[0230]

Fig. 37 is a cross sectional view showing the constitution of the essential section of a semiconductor device as a fourth comparison example. Also, Fig. 44 is a view showing a semiconductor device which is a forth comparison example and illustrates the structure of its substantial part. Further, Fig. 37 shows a sectional view taken along lines A-B in Fig. 44.

[0231]

In Fig. 37 and Fig. 44, the same numeral is

assigned to each of the same components as those shown in Fig. 28.

[0232]

The constituent difference between the aforementioned semiconductor device of the twenty-eighth embodiment (hereinafter, referred to as the twenty-eighth embodiment device again) and the semiconductor device of the fourth comparison example (hereinafter, referred to as the fourth comparison example device) is only a point that with respect to the constitution of the respective end areas of the semiconductor element protective layer 7 and the conductor protective layer 5, the twenty-eighth embodiment device is structured so that the semiconductor element protective layer 7 and the conductor protective layer 5 respectively have slit portions reaching the bottom of the semiconductor element protective layer 7 and the bottom of the conductor protective layer 5, thereby the end face of the conductor protective layer 5 is positioned on the outside compared with the end face of the semiconductor element protective layer 7, and the end face of the conductor protective layer 5 is formed inside the cutting scribe line formed on a semiconductor wafer, and the end surface 1(1) of the

semiconductor element 1 is exposed within the range from the end face to the inside of the scribe line, while the fourth comparison example device is structured so that the end face of the semiconductor element protective layer 7 and the end face of the conductor protective layer 5 are respectively installed on the same plane as that of the end face of the semiconductor element 1 and the semiconductor element 1 has no exposed end surface 1(1) and there are no other constituent differences between the twenty-eighth embodiment device and the fourth comparison example device. Therefore, additional explanation on the constitution of the fourth comparison example device will be omitted.

[0233]

The manufacturing method of the fourth comparison example device is the same as the manufacturing method of the twenty-eighth embodiment device, so that the explanation on the manufacturing method of the fourth comparison example device will be omitted.

[0234]

In the semiconductor devicees of the fourth comparison example manufactured by such a manufacturing method, at the first evaluation time, defective conductor patterns of about 30% are

generated for the lead wire portion 4, and at the second evaluation (appearance inspection) time immediately after dicing, defective semiconductor devicees of about 30% are generated during dicing, and furthermore, at the third evaluation time after the temperature test, package defects such as a disconnection defect are generated in almost all samples.

[0235]

As mentioned above, as compared with the semiconductor devicees of the first to fourth comparison examples, the semiconductor devicees of the first to thirty-third embodiments are structured so that the respective end faces of the stress cushioning layer 3 and the conductor protective layer 5 or the respective end faces of the semiconductor element protective layer 7, the stress cushioning layer 3, and the conductor protective layer 5 are formed inside the scribe line inside the end face of the semiconductor element 1, so that a semiconductor wafer can be cut by surely recognizing the positioning marks put on the semiconductor wafer during cutting of the semiconductor wafer, and occurrences of defective semiconductor packages due to variations of the cutting position of each of the obtained semiconductor

devicees can be eliminated.

[0236]

In the semiconductor devicees of the first to thirty-third embodiments, when each semiconductor device is to be obtained by cutting a semiconductor wafer, the cut portion of each semiconductor device is formed as a single-layer structure of only a semiconductor elementso that even if mechanical stress is generated during cutting of the semiconductor wafer, the mechanical stress is just applied to the single-layer structure and a plurality of resin layers can be prevented from peeling off due to the mechanical force.

[0237]

Furthermore, in the semiconductor devicees of the first to thirty-third embodiments, even if thermal stress is generated due to great changes in the environmental temperature during mounting of each semiconductor device and the thermal stress is applied to a plurality of resin layers, large mechanical stress is not applied to the plurality of resin layers during cutting of a semiconductor wafer and the plurality of resin layers are little damaged, so that peeling-off of the plurality of resin layers due to the thermal stress does not occur at all or very little.

[0238]

Effects of the Invention

As mentioned above, according to the semiconductor device and semiconductor device manufacturing method of the present invention, the respective end faces of the stress cushioning layer and conductor protective layer or the respective end faces of the semiconductor element protective layer, stress cushioning layer, and conductor protective layer in the end surface area of the semiconductor element are formed inside the semiconductor wafer cutting scribe line and the semiconductor element is exposed within the range from the end face to the inside of the scribe line, so that when the semiconductor wafer is to be cut along the semiconductor wafer cutting scribe line, it can be cut by surely recognizing the positioning marks put on the semiconductor wafer and an effect can be produced such that occurrences of defective semiconductor packages due to variations in the cutting position of each obtained semiconductor device can be eliminated.

[0239]

According to the semiconductor device and semiconductor device manufacturing method of the present invention, when each semiconductor device is to be obtained by cutting a semiconductor wafer, the

cut portion of each semiconductor device is formed as a single-layer structure of only a semiconductor element and even if mechanical stress is generated during cutting of the semiconductor wafer, the mechanical stress is just applied to the single-layer structure, so that an effect can be produced such that a plurality of resin layers will not be peeled off by the mechanical force.

[0240]

Furthermore, according to the semiconductor device and semiconductor device manufacturing method of the present invention, even if thermal stress is generated due to great changes in the environmental temperature during mounting of each semiconductor device and the thermal stress is applied to a plurality of resin layers, large mechanical stress is not applied to the plurality of resin layers during cutting of a semiconductor wafer and the plurality of resin layers are little damaged, so that an effect can be produced such that the plurality of resin layers will be peeled off not at all or very little by the thermal stress.

[0241]

As a result, according to the semiconductor device and semiconductor device manufacturing method of the present invention, an effect can be produced such that

each semiconductor device is damaged not at all or very little by application of mechanical stress and thermal stress, and the reliability of semiconductor devicees can be enhanced, and the yield rate during manufacturing of semiconductor devicees can be improved.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a stress cushioning layer installed on said semiconductor elements, a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad, external electrodes arranged on said lead wire portion on said top of said stress cushioning layer, and a conductor protective layer installed on said stress cushioning layer excluding said external electrode arranged portion and on a conductor portion, wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said scribe line.

2. A semiconductor device according to Claim 1, wherein said end face of said conductor protective

player is formed inside said end face of said stress cushioning layer.

3. A semiconductor device according to Claim 1, wherein said end face of said conductor protective player is formed outside said end face of said stress cushioning layer.

4. A semiconductor device according to any of Claims 1 to 3, wherein an end area of said stress cushioning layer is formed so as to become taperingly thinner toward the said end face.

5. A semiconductor device comprising semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a semiconductor element protective layer installed on said semiconductor elements, a stress cushioning layer installed on said semiconductor element protective layer, a first opening formed in said semiconductor element protective layer on said electrode pad, a second opening formed in said stress cushioning layer on said electrode pad, a lead wire portion extending to a top of said stress cushioning layer through said

first opening and said second opening respectively from said electrode pad, external electrodes arranged on said lead wire portion on said top of said stress cushioning layer, and a conductor protective layer installed on said stress cushioning layer excluding said external electrode arranged portion and on said conductor portion, wherein said semiconductor element protective layer, said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside a cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said scribe line.

6. A semiconductor device according to Claim 5, wherein said end face of said conductor protective player is formed inside said end face of said stress cushioning layer.

7. A semiconductor device according to Claim 5, wherein said end face of said conductor protective player is formed outside said end face of said stress cushioning layer.

8. A semiconductor device according to Claim 6 or 7, wherein said end face of said semiconductor element protective player is formed outside said end face of said stress cushioning layer.

9. A semiconductor device according to Claim 6 or 7, wherein said end face of said semiconductor element protective player is formed inside said end face of said stress cushioning layer.

10. A semiconductor device according to any of Claims 4 to 9, wherein an end area of said stress cushioning layer is formed so as to become taperingly thinner toward the said end face.

11. A semiconductor device manufacturing method comprising a first step of forming a plurality of semiconductor elements having an integrated circuit and an electrode pad on a circuit forming surface of a semiconductor wafer, a second step of forming a stress cushioning layer on a plurality of semiconductor elements, a third step of forming an opening in an electrode pad of said stress cushioning layer and forming a notch wider than a width of a scribe line in

said stress cushioning layer on said cutting scribe line of said semiconductor wafer, a fourth step of forming a lead wire portion extending from said electrode pad to said stress cushioning layer via said opening, a fifth step of forming a conductor protective layer which covers said stress cushioning layer and said lead wire portion and has an external electrode connection window portion on said lead wire portion and a notch at a position corresponding to a notch of said stress cushioning layer, a sixth step of forming an external electrode in said external electrode connection window portion, and a seventh step of cutting said semiconductor wafer along said cutting scribe line and obtaining a plurality of semiconductor devicees in minimum units.

12. A semiconductor device manufacturing method according to Claim 11, wherein an end face obtained by said notch of said conductor protective layer at said Step 5 is formed inside said semiconductor wafer cutting scribe line.

13. A semiconductor device manufacturing method according to Claim 12, wherein said end face obtained by said notch of said conductor protective layer at

said Step 5 is formed inside an end face formed by said notch of said stress cushioning layer.

14. A semiconductor device manufacturing method according to Claim 12, wherein said end face obtained by said notch of said conductor protective layer at said Step 5 is formed outside an end face formed by said notch of said stress cushioning layer.

15. A semiconductor device manufacturing method comprising a first step of forming a plurality of semiconductor elements having an integrated circuit and an electrode pad on a circuit forming surface of a semiconductor wafer, a second step of forming a semiconductor element protective layer on a plurality of semiconductor elements, a third step of forming a first opening in an electrode pad of said semiconductor element protective layer and forming a notch wider than a width of a scribe line in said semiconductor element protective layer on said cutting scribe line of said semiconductor wafer, a fourth step of forming a stress cushioning layer on said semiconductor element protective layer, a fifth step of forming a second opening in said electrode pad of said stress cushioning layer and forming a notch at a

position corresponding to a notch of said semiconductor element protective layer in said stress cushioning layer on said cutting scribe line of said semiconductor wafer, a sixth step of forming a lead wire portion extending from said electrode pad to said stress cushioning layer via said first opening and said second opening, a seventh step of forming a conductor protective layer which covers said stress cushioning layer and said lead wire portion and has an external electrode connection window portion on said lead wire portion and a notch at a position corresponding to said notch of said stress cushioning layer, an eighth step of forming an external electrode in said external electrode connection window portion, and a ninth step of cutting said semiconductor wafer along said cutting scribe line and obtaining a plurality of semiconductor devicees in minimum units.

16. A semiconductor device manufacturing method according to Claim 15, wherein an end face obtained by said notch of said stress cushioning layer at said Step 4 is formed inside said semiconductor wafer cutting scribe line.

17. A semiconductor device manufacturing method

according to Claim 16, wherein said end face obtained by said notch of said stress cushioning layer at said Step 4 is formed inside an end face formed by said notch of said semiconductor element protective layer.

18. A semiconductor device manufacturing method according to Claim 16, wherein said end face obtained by said notch of said stress cushioning layer at said Step 4 is formed outside an end face formed by said notch of said semiconductor element protective layer.

19. A semiconductor device manufacturing method according to Claim 16, wherein said end face obtained by said notch of said stress cushioning layer at said Step 4 is formed so as to be installed on the same plane as that of an end face formed by said notch of said semiconductor element protective layer.

20. A semiconductor device manufacturing method according to Claim 15, wherein an end face obtained by said notch of said conductor protective layer at said Step 7 is formed inside said semiconductor wafer cutting scribe line.

21. A semiconductor device manufacturing method

according to Claim 20, wherein said end face obtained by said notch of said conductor protective layer at said Step 7 is formed inside an end face formed by said notch of said semiconductor element protective layer.

22. A semiconductor device manufacturing method according to Claim 20, wherein said end face obtained by said notch of said conductor protective layer at said Step 7 is formed outside an end face formed by said notch of said semiconductor element protective layer.

23. A semiconductor device manufacturing method according to Claim 20, wherein said end face obtained by said notch of said conductor protective layer at said Step 7 is formed so as to be installed on the same plane as that of an end face formed by said notch of said semiconductor element protective layer.

24. A semiconductor device manufacturing method according to Claim 16 or 20, wherein said end face obtained by said notch of said conductor protective layer at said Step 7 is formed inside an end face formed by said notch of said semiconductor element

protective layer and an end face formed by said notch of said stress cushioning layer.

25. A semiconductor device manufacturing method according to Claim 16 or 20, wherein said end face obtained by said notch of said conductor protective layer at said Step 7 is formed outside an end face formed by said notch of said semiconductor element protective layer and an end face formed by said notch of said stress cushioning layer.

26. A semiconductor device manufacturing method according to Claim 16 or 20, wherein said end face obtained by said notch of said conductor protective layer at said Step 7 is formed between an end face formed by said notch of said semiconductor element protective layer and an end face formed by said notch of said stress cushioning layer.

27. A semiconductor device manufacturing method according to Claim 16 or 20, wherein said end face obtained by said notch of said conductor protective layer at said Step 7 is formed to be installed on the same plane as that of an end face formed by said notch of said semiconductor element protective layer and an

end face formed by said notch of said stress cushioning layer.

ABSTRACT

The present invention is a semiconductor device having the semiconductor element 1 obtained by cutting a semiconductor wafer with the electrode pad 2 formed on one side along the scribe line, the semiconductor element protective layer 7 on the semiconductor element 1 which has the opening 7(1) on the pad 2, the stress cushioning layer 3 on the layer 7 which has the opening 3(1) on the pad 2, the lead wire portion 4 reaching the layer 3 from the electrode pad 2 via the openings 7(1) and 3(1), the external electrodes 6 on the lead wire portion 4, and the conductor protective layer 5 on the layer 3 and the layer 7, the layer 3, and the conductor protective layer 5 form the respective end faces on the end surface 1(1) of the semiconductor element 1 inside the scribe line and expose the range from the end face of the end surface 1(1) to the inside of the scribe line.